signal indicative thereof;

a second place shifting device that includes a second logical assignment circuit to shift data bits of said received multiplicant~~d~~ in response to a second shift command signal, and provides a second shifted signal indicative thereof;

means for summing said first and second shifted signals to provide a summed signal value that is indicative of the product of said multiplier and said multiplicant~~d~~; and

a control device that receives a signal indicative of said multiplier, and generates said first and second shift command signals indicative of said multiplier value.

2.(Original) The computing device of claim 1, comprising a memory device for storing said summed signal, and for providing past values of said summed signal value.

3.(Original) The computing device of claim 2, wherein said means for summing receives and sums a signal value from said memory device indicative of a past value of said summed signal value with said first and second shifted signals to provide said summed signal value.

4.(Currently Amended) The computing device of claim 1, wherein said first place shifting device comprises a first sign inverter that receives and inverts the sign of said received multiplicant~~d~~ to provide a sign inverted received multiplicant~~d~~ signal that is input to said first logical assignment circuit for bit shifting.

5.(Currently Amended) The computing device of claim 4, wherein said second place shifting device comprises a second sign inverter that receives and selectively inverts the sign of said received

multiplicant~~d~~ to provide a second sign inverted received multiplicant~~d~~ signal that is input to said second logical assignment circuit for bit shifting.

6.(Original) The computing device of claim 1, wherein said control unit generates a first sign inversion command signal in response to said multiplier value, wherein said first sign inversion signal is input to said first sign inverter to selectively enable the sign inversion.

7.(Currently Amended) A computing device on a monolithic integrated circuit for multiplying together a digitized multiplier signal value and a digitized multiplicant~~d~~ signal value, said computing device comprising:

an input interface that receives said multiplicant~~d~~ and provides a received multiplicant~~d~~ indicative thereof;

first means for shifting data bits of said received multiplicant~~d~~ in response to a first shift command signal, and for providing a first shifted signal indicative thereof;

second means for shifting data bits of said received multiplicant~~d~~ in response to a second shift command signal, and for providing a second shifted signal indicative thereof;

means for summing said first and second shifted signals to provide a summed signal value that is indicative of the product of said multiplier and said multiplicant~~d~~; and

a control device that receives a signal indicative of said multiplier that is a binary coded number using canonical form, and generates said first and second shift command signals indicative of said multiplier value.

8.(Original) The computing device of claim 7, comprising a memory device for storing said

summed signal, and for providing past values of said summed signal value.

9.(Original) The computing device of claim 8, wherein said means for summing receives and sums a signal value from said memory device indicative of a past value of said summed signal value with said first and second shifted signals to provide said summed signal value.

10.(Currently Amended) The computing device of claim 7, wherein said first means for shifting comprises a first sign inverter that receives and inverts the sign of said received multiplicant~~d~~d to provide a sign inverted received multiplicant~~d~~d signal that is input to said first logical assignment circuit for bit shifting.

11.(Currently Amended) The computing device of claim 10, wherein said second means for shifting comprises a second sign inverter that receives and selectively inverts the sign of said received multiplicant~~d~~d to provide a second sign inverted received multiplicant~~d~~d signal that is input to said second logical assignment circuit for bit shifting.

12.(Canceled)

13.(Canceled)

14.(Canceled)

15.(Canceled)

16.(Canceled)

17.(Canceled)

18.(Canceled)